CLAIMS

What is claimed is:

1   1.   An apparatus, comprising:

2   a first interface;

3   a second interface not directly coupled to said first interface; and

4   a cache accessible from said first interface and said second

5   interface, to contain a cache line with a first cache coherency state

6   when accessed from said first interface and a second cache coherency

7   state when accessed from said second interface.

1   2.   The apparatus of claim 1, wherein said first cache

2   coherency state has higher privilege than said second cache coherency

3   state when said second interface is coupled to a processor.

1   3.   The apparatus of claim 2, wherein said second cache

2   coherency state is to reduce snoop transactions on said second

3   interface.

1   4.   The apparatus of claim 2, wherein said first cache

2   coherency state is exclusive and said second cache coherency state is

3   shared.

1   5.   The apparatus of claim 2, wherein said first cache

2   coherency state is modified and said second cache coherency state is

3   shared.

1   6.   The apparatus of claim 3, wherein said second cache

2   coherency state supports speculative invalidation.

1   7.   The apparatus of claim 6, wherein said first cache
2 coherency state is modified and said second cache coherency state is
3 invalid.

1   8.   The apparatus of claim 6, wherein said first cache
2 coherency state is exclusive and said second cache coherency state is
3 invalid.

1   9.   The apparatus of claim 6, wherein said first cache
2 coherency state is shared and said second cache coherency state is
3 invalid.

1   10.   The apparatus of claim 6, wherein said second cache
2 coherency state further supports explicit invalidation.

1   11.   A method, comprising:
2   associating a first cache coherency state with a first cache line in
3 a first cache;
4   associating a second cache coherency state with a second cache
5 line in a second cache in an inner relationship to said first cache;
6   transitioning said first cache coherency state to a joint cache
7 coherency state including said first cache coherency state for outer
8 interfaces and a third cache coherency state for inner interfaces; and
9   transitioning said second cache coherency state to said third
10 cache coherency state.

1   12.   The method of claim 11, wherein said first cache coherency
2 state is exclusive, said second cache coherency state is invalid, and said
3 third cache coherency state is shared.

1   13.   The method of claim 11, wherein said first cache coherency

2   state is modified, said second cache coherency state is modified, and

3   said third cache coherency state is invalid.

1   14.   A method, comprising:

2   associating a first cache coherency state with a first cache line in

3   a first cache;

4   associating a second cache coherency state with a second cache

5   line in a second cache in an inner relationship to said first cache;

6   transitioning said second cache coherency state to an invalid

7   state; and

8   transitioning said first cache coherency state to a joint cache

9   coherency state including said first cache coherency state for outer

10 interfaces and an invalid state for inner interfaces.

1   15.   The method of claim 14, wherein said first cache coherency

2   state is modified.

1   16.   The method of claim 14, wherein said first cache coherency

2   state is exclusive.

1   17.   The method of claim 14, wherein said first cache coherency

2   state is shared.

1   18.   A method, comprising:

2   associating a first cache coherency state with a first cache line in

3   a first cache;

4   associating an invalid state with a second cache line in a second

5   cache in an inner relationship to said first cache;

6   transitioning said invalid state to a shared state; and

7   transitioning said first cache coherency state to a joint cache

8   coherency state including a shared state for inner interfaces.

1   19.   The method of claim 18, wherein said first cache coherency
2   state is invalid and said joint cache coherency state is exclusive-shared.

1   20.   The method of claim 18, wherein said first cache coherency
2   state is modified-invalid and said joint cache coherency state is
3   modified-shared.

1   21.   An apparatus, comprising:
2   means for associating a first cache coherency state with a first
3   cache line in a first cache;
4   means for associating a second cache coherency state with a
5   second cache line in a second cache in an inner relationship to said
6   first cache;
7   means for transitioning said first cache coherency state to a joint
8   cache coherency state including said first cache coherency state for
9   outer interfaces and a third cache coherency state for inner interfaces;
10 and
11   means for transitioning said second cache coherency state to said
12 third cache coherency state.

1   22.   The apparatus of claim 21, wherein said first cache
2   coherency state is exclusive, said second cache coherency state is
3   invalid, and said third cache coherency state is shared.

1   23.   The apparatus of claim 21, wherein said first cache
2   coherency state is modified, said second cache coherency state is
3   modified, and said third cache coherency state is invalid.

1   24.   An apparatus, comprising:

2   means for associating a first cache coherency state with a first

3 cache line in a first cache;

4   means for associating a second cache coherency state with a

5 second cache line in a second cache in an inner relationship to said

6 first cache;

7   means for transitioning said second cache coherency state to an

8 invalid state; and

9   means for transitioning said first cache coherency state to a joint

10 cache coherency state including said first cache coherency state for

11 outer interfaces and an invalid state for inner interfaces.

1   25.   The method of claim 24, wherein said first cache coherency

2 state is modified.

1   26.   The method of claim 24, wherein said first cache coherency

2 state is exclusive.

1   27.   The method of claim 24, wherein said first cache coherency

2 state is shared.

1   28.   An apparatus, comprising:

2   means for associating a first cache coherency state with a first

3 cache line in a first cache;

4   means for associating an invalid state with a second cache line in

5 a second cache in an inner relationship to said first cache;

6   means for transitioning said invalid state to a shared state; and

7   means for transitioning said first cache coherency state to a joint

8 cache coherency state including a shared state for inner interfaces.

Assignee: Intel Corporation

1   29.   The apparatus of claim 28, wherein said first cache
2 coherency state is invalid and said joint cache coherency state is
3 exclusive-shared.

1   30.   The apparatus of claim 28, wherein said first cache
2 coherency state is modified-invalid and said joint cache coherency state
3 is modified-shared.

1   31.   A system, comprising:
2   a cache accessible from a first interface and a second interface, to
3 contain a cache line with a first cache coherency state when accessed
4 from said first interface and a second cache coherency state when
5 accessed from said second interface;
6   a bus bridge to a third interface; and
7   an input-output device coupled to said third interface.

1   32.   The system of claim 31, wherein said first cache coherency
2 state has higher privilege than said second cache coherency state when
3 said second interface is coupled to a processor.

1   33.   The system of claim 31, wherein said second cache
2 coherency state is to reduce snoop transactions on said second
3 interface.